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Performance response improvement of power electronics converter using cascade controllers

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Abstract

In various areas of electrical and electronic equipment applications, power electronic converters are widely used. However, the fast and nonlinear dynamics are associated with these converters. Thus, designing a controller with high response speed and robust capability is critical to guarantee efficient operation of a power electronic converter. A computer-based model was developed in the MATLAB/Simulink environment. The high overshoot experienced can be attributed to the inability of the buck converter to handle nonlinearity in the system's dynamic process. To address this challenge and improve system performance, a Proportional-Integral-Derivative (PID) controller was designed and integrated into the converter's control loop. Simulation results indicated that the application of the PID controller led to faster response and shorter convergence time, measured by rise time (3.01e-05 s) and settling time (0.000223 s), along with better stability and a smoother response, evidenced by the reduction of overshoot from 42.3% to 10.9%. Therefore, a cascade control system based on combined Fuzzy-PID and PID controllers was designed and applied to the buck converter. The simulation results showed that the cascade control scheme achieved an improved rise time of 1.88 × 10^(-5) s, a settling time of 3.02 × 10^(-5) s, and an overshoot of 1.36%.

Keywords: Cascaded system, Control system, DC-to-DC converter, Fuzzy logic, Performance-response, PID-controllers, Power electronics.

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Contents

Contribution of this paper to the literature
The contribution of this work to the body of knowledge is the design and application of a buck converter cascade control system based on combined Fuzzy-PID and PID controllers, which provides intelligence and faster system performance control response.

1. Introduction

A power electronic converter basically consists of different sub-systems such as capacitors, power modules, control units, gate drivers, and a cooling system [1]. Though none of these sub-systems are perfect and can fail over time, they can affect system operation [2]. The two most fragile components are the power modules and electrolytic capacitors, which are also prone to wear-out failure [1]. Their reliability depends on factors such as the mechanical strength of the device, applied electric load, climate conditions, control, and switching techniques. The material composition of these components degrades over long-term operation of the converter, eventually causing potential failure mechanisms [1]. Types of DC-to-DC converters.

1.1. Boost Converter

The Boost Converter is a step-up DC/DC voltage converter operating in the second quadrant. The output voltage increases in an arithmetic progression. It has limitations on the DC link voltage level and the complexity of the control circuit. Figure 1 shows a circuit diagram of a typical boost converter.

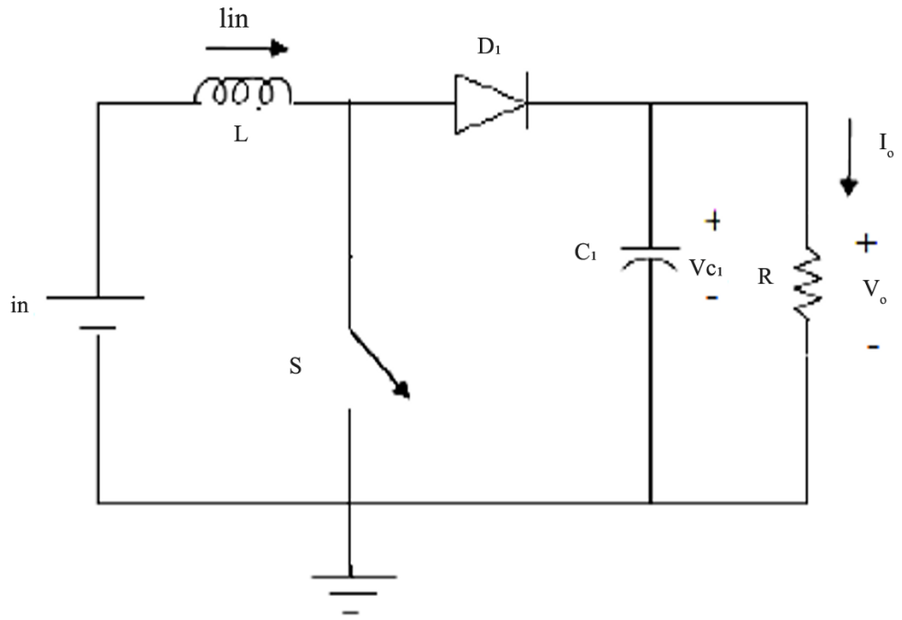

Figure 1. Boost converter.
Source: Gunasekaran [3].

The circuit analysis is established in Figure 1 for the output voltage, Vo, average output current, Io, voltage transfer gain across capacitor Vc1, resistor R, diode D1, inductor L, capacitor C1, ripple current in the inductor Lin, and duty cycle of conduction period T as follows (1).

$$V_o = \frac{T}{T - t_{on}} V_{in} \quad (1)$$

1.1.1. Non-Isolated Buck-Boost Converter

A typical buck-boost converter is shown in Figure 2. The circuit operation is presented based on the analysis in (3).

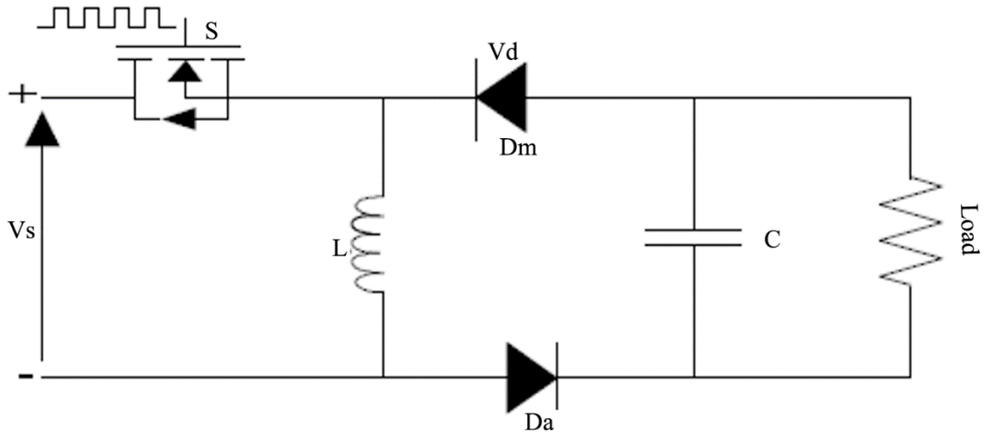

Figure 2. Non-isolated buck-boost converter.
Source: Dogra and Pal [4].

The circuit operates in two modes. Switch closed operation (Mode 1): When the switch is closed, the diodes D_m and D_a are in reverse-bias mode. The input current increases, flows through inductor L, and switch S. This causes energy to accumulate in inductor L. The capacitor C discharges through load R.

Switch open operation (Mode 2): When the switch is open, the current flowing through inductor L would flow through L, C, D_a, D_m, and the load. The energy stored in inductor L would be transferred to the capacitor and load; inductor current would fall until transistor switch Q is switched on again in the next cycle [4].

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{1}{L} V_{in} \\ \dfrac{dV_{out}}{dt} = \dfrac{1}{C}\left(-\dfrac{V_{out}}{R}\right) \end{cases}, 0 < t < dT, Q: ON \qquad (2)$$

and with the switch in OFF state:

$$\begin{cases} \dfrac{di_L}{dt} = \dfrac{1}{L} V_{out} \\ \dfrac{dV_{out}}{dt} = \dfrac{1}{C}\left(-i_L - \dfrac{V_{out}}{R}\right) \end{cases}, dT < t < T, Q: OFF \qquad (3)$$

The buck-boost converters have pulsating output current and require current handling capability. To overcome these drawbacks, the Luo converter is used; it can reduce ripple voltage and current levels without inverting the polarities [5].

1.1.2. Voltage Lift Converters

The first three stages of Positive Output Super-Lift Converters are presented here. They are the Elementary (Self-Luo) circuit, the Re-Lift circuit, and the Triple-Lift circuit, respectively. These circuits are shown in Figures 3 to 4.

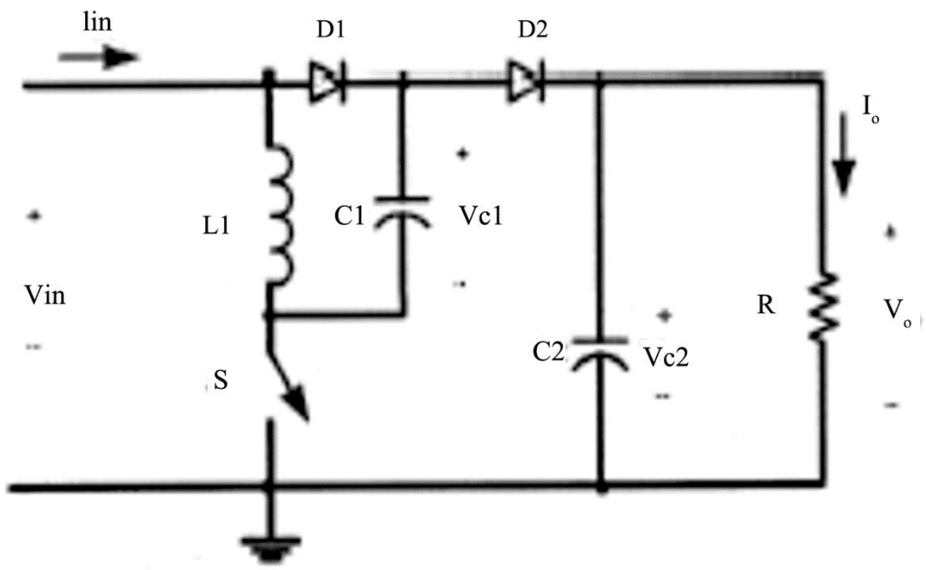

Figure 3. Schematic diagram of a self-lift converter.

Source: Prasanna et al. [6].

1.1.3. Self-Lift Circuit

This converter (Figure 2) consists of V_{in} =input voltage, capacitors C_1 and C_2 inductor L, power switch S and freewheel diodes D_1 and D_2, R=resistance, Io=output current, Vo=output voltage, VC1=voltage across capacitor C1, VC2=voltage across capacitor C2. Also, it has a voltage lift circuit (VLC). VLC consists of diode D_1 and capacitor C_1. Switch S and diode D are alternately on and off. Usually, this pump operates in continuous mode; the inductor current remains continuous. The output terminal voltage and current are typically positive. In this positive Luo converter, it is important to note that there are two states: when the switch is on and when it is off [1, 7].

The Voltage across capacitor $C_1$is charged toV_{in}. The current I_{L_1} flowing through inductor L_1 increases with voltage V_{in} during the switching-on period kT and decreases with voltage $-(V_o - 2V_{in})$ during the switching-off period $(1-K)T$. Therefore [6].

$$KTV_{in} - (1-K)T \times (V_o - 2V_{in}) = 0 \qquad (4)$$

The output voltage can be calculated from Equation 4, and is given by:

$$V_o = \left(\frac{2-K}{1-K}\right) V_{in} \qquad (5)$$

The analysis of the self-lift circuit converter for output voltage, average output current, voltage transfer gain, and ripple current in the inductor is given in terms of the duty cycle of the conduction period G by Gunasekaran [3].

$$V_o = \left(\frac{2-G}{1-G}\right) V_{in} \qquad (6)$$

$$I_o = \left(\frac{2-G}{1-G}\right) I_{in} \quad (7)$$

$$K = \frac{V_o}{V_{in}} = \frac{2-G}{1-G} \quad (8)$$

$$\delta I = \left(\frac{V_o - 2V_{in}}{L}\right) t_{off} \quad (9)$$

$$G = \frac{t_{on}}{t_{on} + t_{off}} = \frac{t_{on}}{T} \quad (10)$$

1.1.4. Re-Lift Circuit

To derive the Re-Lift circuit, the parts (L_2-D_3-D_4-D_5-C_3-C_4) of the Elementary circuit are added. The circuit diagram of a re-lift DC-DC converter is shown in Figure 4.

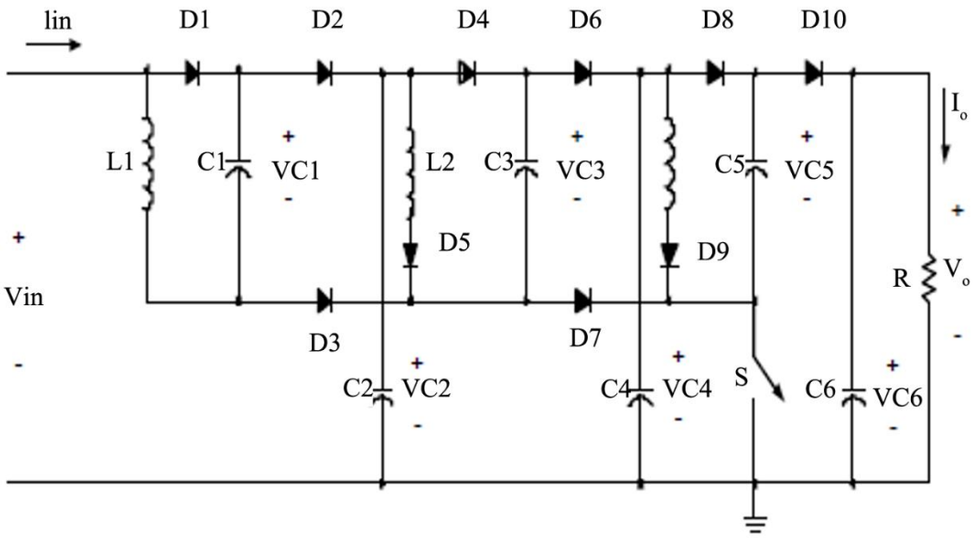

Figure 4. Schematic diagram of the re-lift converter.

Source: Luo and Ye [8].

The voltage across capacitor C_1 is charged to V_{in}. As described above for the elementary (self-lift) circuit, the voltage V_{C2} across capacitor C_2 is given by:

$$V_{C2} = \frac{2-K}{1-K} V_{in} \quad (11)$$

The voltage across capacitor C_3 is charged to V_{C2}. The current flowing through inductor L_2 increases with Voltage V_{C2}during the switching-on period k and decreases with voltage – (V_o-2V_{C2}) during the switching-off period (1-k) T. Therefore, the output voltage V_o across capacitor C_4 is:

$$KTV_{C2} - (1-K)T(V_o - 2V_{C2}) = 0 \quad (12)$$

$$V_o = \left(\frac{2-K}{1-K}\right) V_{C2} = \left(\frac{2-K}{1-K}\right)^2 V_{in} \quad (13)$$

The voltage across capacitor C_1 is charged to V_{in}. As described before, the voltage across capacitor C_2 is charged to V_{C2} as given by Equation 13, and the voltage across capacitor is charged to:

$$V_{C4} = V_o = \left(\frac{2-K}{1-K}\right)^2 V_{in} \quad (14)$$

The voltage across capacitor C_5 is charged to V_{C4}. The current flowing through inductor L_3 increases with voltage V_{C4} during the switching-on period and decreases with voltage – (V_o–2V_{C4}) during switching-off (1–k) T. Therefore, the output voltage V_o across capacitor C_6 is:

$$KTV_2 = (1-K)T(V_o - 2V_{C4}) \quad (15)$$

$$V_o = \left(\frac{2-K}{1-K}\right) V_{C4} = \left(\frac{2-K}{1-K}\right)^2 V_{C2} = \left(\frac{2-K}{1-K}\right)^3 V_{in} \quad (16)$$

Prasanna et al. [6] designed and analyzed a positive output lift Luo (POTLLC). They stated that the proposed system was characterized by robustness around the operating point, good transient response performance under changing operating conditions and/or input voltage, and invariant dynamic performance under varying conditions. They maintained that the converter could perform voltage conversion from a positive source voltage to a positive load voltage. The entire system was implemented in MATLAB/Simulink. In their work, no control circuit was implemented; rather, the system was examined in its conventional state.

Dhanasekar and Kayalvizhi [9] developed a fuzzy logic controller as the control system for the converter. It stated that the performance of the triple lift Luo converter with the fuzzy logic controller was evaluated in the presence of line and load disturbances using MATLAB/Simulink-based simulation. It maintained that the results

achieved were satisfactory and that the fuzzy logic controller effectively rejected the line and load disturbances. Despite the performance, systems with fuzzy logic alone are prone to steady-state error.

Achebe and Muoghalu [10] and Muoghalu and Achebe [11] designed an adaptive PD controller for a microsatellite yaw axis attitude control system, showcasing the varied usage of proportional-derivative controllers and their effective control methods.

Achebe and Muoghalu [10] and Muoghalu and Achebe [11] proposed the enhancement of the dynamic response servo positioning system using an internal model control-based compensator demonstrates how the internal system controller is managed and improved in servo positioning.

Jayachandran et al. [7] analyzed open-loop power stage dynamics relevant to voltage mode control for an elementary (self-lift) Luo DC-DC converter, which is examined for applications such as Hybrid Electric Vehicles (HEV) and fuel cell vehicles (FCV). A comparative analysis of the output super lift series of converters was conducted to evaluate voltage gain, output voltage ripple, stresses on the switches, and efficiency. The most suitable converter from the series was modeled and verified using the state space average method and circuit average technique. A transfer function was derived for both output and input voltages, indicating that this function could be used to model the complete Luo converter with voltage mode control. Modeling was performed in MATLAB/Simulink and used for simulation to confirm the predicted results. This work focused solely on modeling a Luo-type DC-DC converter and examining its performance in an open-loop state.

Muoghalu et al. [12] developed a human heartbeat stabilizer using controllers based on proportional-integral-derivative, which is an exposition on PID controller usage. It improved response stabilization and control techniques.

Suguna et al. [5] developed a super lift Luo converter to boost power from PV cells. It stated that many maximum power point (MPP) techniques exist for extracting maximum power from PV cells, differing in convergence speed, simplicity, sensors, hardware implementation, cost, and acceptability. An improved perturb and observe (MPP) technique combined with a super lift Luo converter was implemented. The circuit was modeled and simulated using MATLAB software. By using the super lift Luo converter and the improved perturb and observe algorithm for PV cells, a high output was obtained.

Muoghalu et al. [12] developed state-space modeling and control of a two-phase hybrid stepping motor for robot grinding using an LQR controller, revealing various methods for improving dynamic response and controllers.

Vijay and Palwalia [13] presented a novel analysis and modeling of a boost and buck converter. They modeled and simulated a non-isolated DC-DC boost and buck converter using a PI controller. The boost converter was designed for 12 V to 24 V with an output current of 1 A at a switching frequency of 100 kHz. The buck converter was similarly designed for 24 V to 12 V with an output current of 0.86 A at a switching frequency of 100 kHz. They concluded that the system's performance could be improved by tuning the PI controller parameters for a better response of the DC-DC converter.

Muoghalu et al. [12] designed a linear slip control for an improved anti-lock braking system, outlining the procedures for controlling slip in the brake system. It fully explained the linear control methods used in brake control of a system in motion.

2. Research Gaps

Despite the breadth of research, several gaps remain.

i. Limited experimental validation—most studies present only simulation results of a single loop, but prototype testing is scarce, leaving real-world performance under component tolerances and electromagnetic interference uncertain.
ii. Handling of non-minimum-phase dynamics—converters with right-half-plane zeros, such as buck-boost—are addressed with complex cascade structures, but stability guarantees and robust performance analyses remain underexplored.
iii. Wide-range operating conditions – Few works examine controller robustness across the full envelope of input voltage and load variations, particularly for Luo-type converters.
iv. Hybrid fuzzy-PID implementations – Although fuzzy logic has been applied to Luo converters, a combined fuzzy-PID architecture that exploits both interpretability and integral action has not been thoroughly investigated; hence, the aim of this project work.

3. Methodology

3.1. Materials

The tools used in this work to realize the main objective are presented in the MATLAB m-file environment.

MATLAB Control System Tool Manager, graphical user interface (GUI) of PID-Tuning compensator, and fuzzy logic embedded block.

3.2. Method

The existing control loop for the buck converter, based on a single-loop control technique using a PID controller, is shown in Figure 5. In the figure, the entire control is provided by a single loop based on the error between the output voltage and the reference voltage, without considering the state of the other electrical quantity (current) at the output. This control model does not guarantee stable, robust, and reliable operation for the power electronic system. Therefore, an approach that addresses the performance limitations of single-loop control through a multi-loop strategy is developed in this work for the buck converter. The cascade control system developed in this work is shown in Figure 6. The steps taken in modeling the cascade control system are presented in the subsequent subsections.

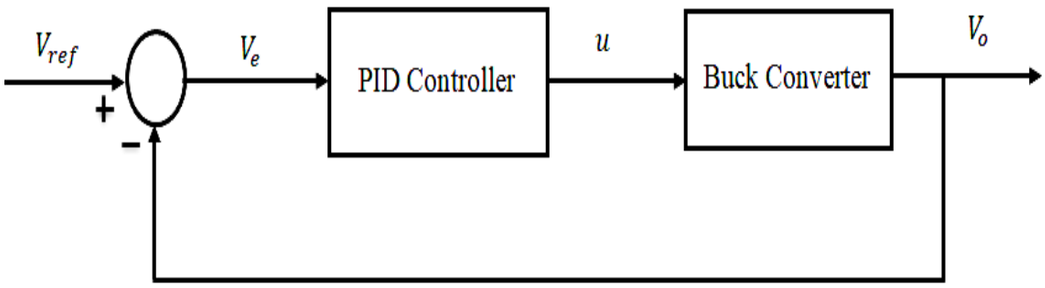

Figure 5. Single-loop PID control buck converter.

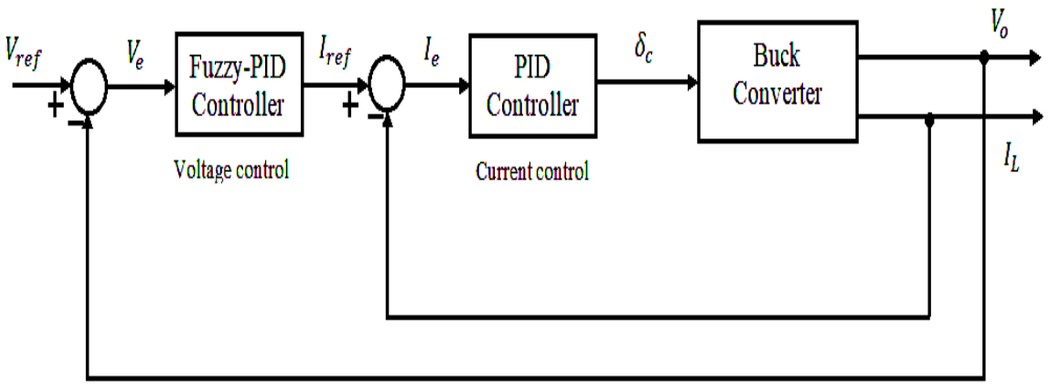

Figure 6. Cascade control system for buck converter.

A power electronic converter, a buck converter, supplies a load with a DC voltage lower than the supply voltage. This work designs a switch-mode buck converter model to regulate voltage from 48 V to 12 V. The switching frequency of the buck converter is set at 100 kHz. The cascade control system is designed in a manner that the inductor current, $I_L$is controlled by the inner loop controller, while the outer loop controller controls the output voltage, V_o. The current reference signal to the inner current loop is the output of the outer voltage loop. The duty cycle signal δ_c to the pulse width modulation (PWM) block is then provided by the inner current loop.

3.3. Mathematical Model of DC-DC Buck Converter

The task of a buck converter is to reduce a higher DC voltage to a lower level, achieved by PWM control. The electrical circuit schematic of a buck converter is shown in Figure 7. The circuit includes a power electronic switching device (such as a MOSFET) represented as S_m, a diode D, an inductor L, a capacitor C, and a load resistance R. In this arrangement, the inductor provides energy storage. Voltage ripple is minimized by connecting the capacitor to the output end of the circuit.

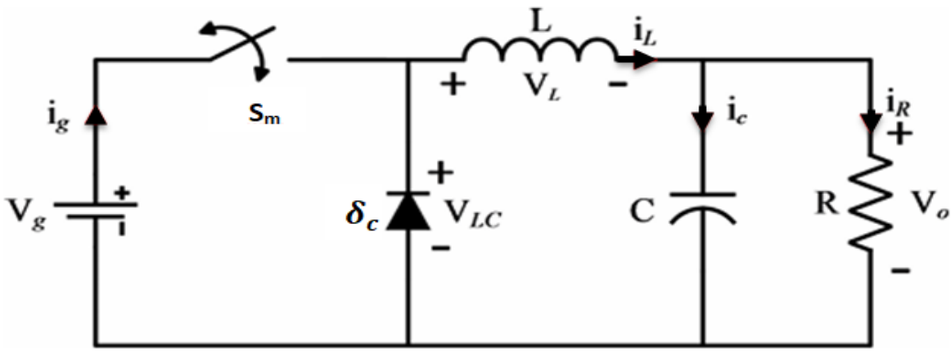

Figure 7. Topology of DC-DC buck converter.

Given the circuit in Figure 7, with an excitation electrical signal of supply voltage V_g and currentI_g. The following relationships are established due to the switching action as defined in Equations 17 and 18.

$$T_{On} = \delta_c T_s \quad (17)$$

$$T_{Off} = (1 - \delta_c)T_s \quad (18)$$

where δ_c is the duty cycle, T_s is the period of a complete switching, T_{on} and T_{off} are the times the switch is on (or closed) and off (or open), respectively. Now, depending on the closed or open mode of the switch S_m, state equations are determined according to Kirchhoff's circuit laws. Thus, for the switch at closed mode and open mode, the state equations are as follows [14].

$$\begin{pmatrix} \hat{i}_L \\ \hat{v}_o \end{pmatrix} = \begin{pmatrix} 0 & -L^{-1} \\ C^{-1} & -(RC)^{-1} \end{pmatrix} \begin{pmatrix} i_L \\ v_o \end{pmatrix} + \begin{pmatrix} L^{-1} \\ 0 \end{pmatrix} v_g \quad (19)$$

$$\begin{pmatrix} \hat{i}_L \\ \hat{v}_o \end{pmatrix} = \begin{pmatrix} 0 & -L^{-1} \\ C^{-1} & -(RC)^{-1} \end{pmatrix} \begin{pmatrix} i_L \\ v_o \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \end{pmatrix} v_g \quad (20)$$

Equations 19 and 20 are the closed and open modes switch state representations, respectively. Assuming zero initial conditions, the transfer function of the buck converter from diode, D (representing the component for achieving switching duty,δ_c) is given in Equation 21.

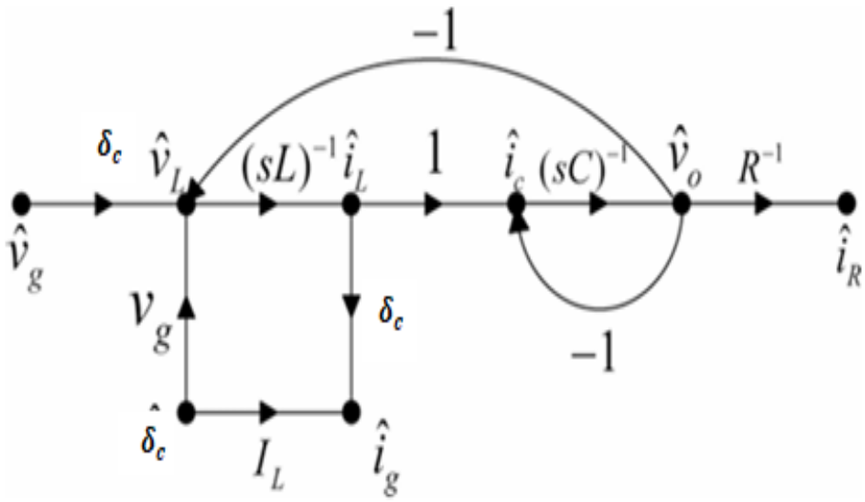

Figure 8. Signal flow graph model of a buck converter.
Source: Jabari et al. [14].

Figure 8 illustrates the signal flow graph model of a buck converter with a feedback loop circuit and a duty cycle in which the output is compared to the reference voltage. This loop stabilizes the regulated output voltage despite load/input changes. The duty cycle δc adjusts the on/off timing of the circuit. The switching action of (L-C) converts the input to the output voltage based on the duty cycle.

$$\frac{V_o(s)}{V_g(s)} = \frac{R\delta_c}{RLCs^2+Ls+R} \quad (21)$$

Where V_o is output voltage, V_g is the supply or input voltage (i.e., reference voltage). The values of the parameters for the buck converter are listed in Table 1. Substituting these values into Equation 21 gives the output voltage in Equation 22.

$$V_o = \left(\frac{216}{6e-07s^2+0.001s+6}\right) \times 1/3 \quad (22)$$

3.4. Design of PID Controller

Figure 9 shows the control system configuration of the PID controller. The mathematical representation of the linear relationship between the controller output, u(t), and the error, e(t), with respect to three-term constants for the three components of the system given in Equation 23.

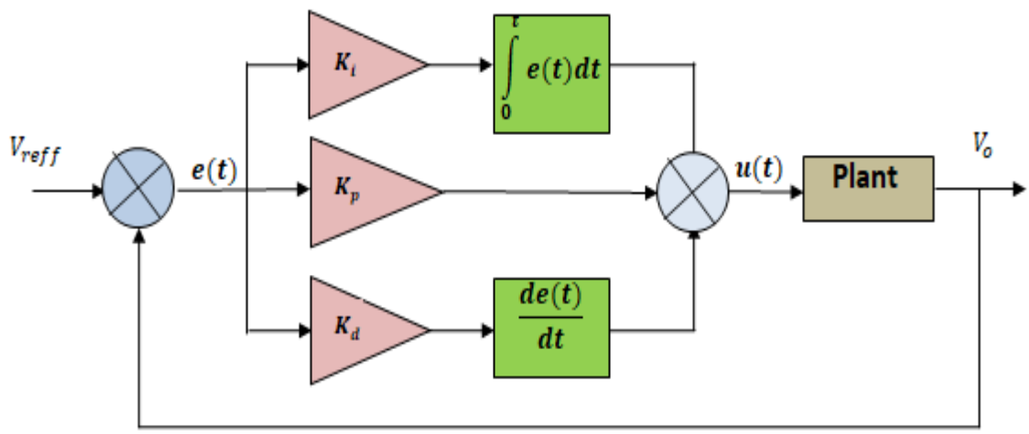

Figure 9. PID Control System Configuration.

$$u(t) = K_p e(t) + K_i \int e(t)dt + K_d \frac{de(t)}{dt} \quad (23)$$

Where $e(t)$ is the error signal, which is the deviation of the output voltage of the converter from the supply input voltage given by:

$$e(t) = V_{reff} - V_o \quad (24)$$

The Laplace transform of Equation 24, assuming zero initial conditions, gives.

$$U(s) = K_p E(s) + K_i \frac{E(s)}{s} + K_d sE(s) \quad (25)$$

Taking the ratio of the control variable, $U(s)$ to the error signal, $E(s)$ gives the PID controller.

$$C_{pid}(s) = \frac{U(s)}{E(s)} = K_p + K_i \frac{1}{s} + K_d \quad (26)$$

The tuned parameters of the PID are proportional gain, K_p = 4.83, integral gain, K_i = 1.34e+04, and derivative gain, K_d = 0.000436. The controller aims to track a setpoint with a rise time of less than 0.5 seconds, an overshoot below 10%, and a steady-state error of essentially zero or close to zero. The parameters were obtained using a two-step approach.

The resulting output voltage of the buck converter with the PID controller, as shown in Figure 9, is given in Equation 26. Further simplification of Equation 27 gives Equation 28.

$$V_{opid} = \frac{\left(4.83+\frac{1.34e+04}{s}+0.000436\right)\times\left(\frac{216}{6e-07s^2+0.001s+6}\right)\times 1/3}{1+\left(4.83+\frac{1.34e+04}{s}+0.000436\right)\times\left(\frac{216}{6e-07s^2+0.001s+6}\right)\times 1/3} \quad (27)$$

$$V_{opid} = \frac{0.09413s^2+1043s+2.888e06}{1.8e-06s^3+0.09713s^2+1061s+2.888e06} \quad (28)$$

3.5. Design Fuzzy Logic Controller

The design and implementation of FLC are carried out in MATLAB/Simulink environment using the Mamdani model, and the method of defuzzification used is the center of gravity. FLC is usually characterized by at least two inputs and one output, with mapping of inputs to output performed by the Mamdani fuzzy inference system (FIS) using membership functions (MFs) of the fuzzy sets. A shape, as shown in Figure 10a-c, illustrates how each point in the input crisp value is associated with a degree of fuzzy value, called a membership function (MF) [15].

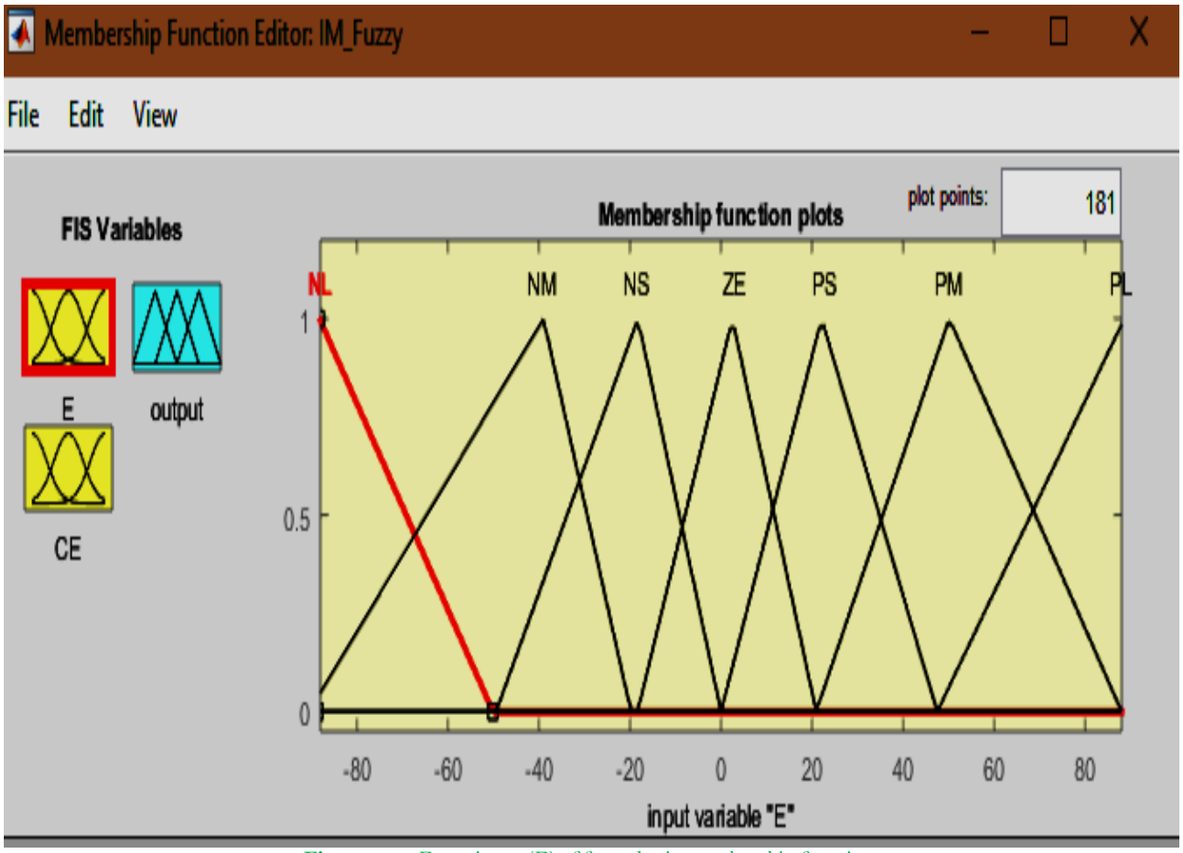

Figure 10a. Error input (E) of fuzzy logic membership function.

In the fuzzy logic system (FLS), the error input (E) is the crisp, numerical difference between a desired reference value (set point) and the actual output of a system (as shown in the triangular control system). The membership function for this error is a curve that defines the degree of truth (a value between 0 and 1) for various linguistic interpretations of that error.

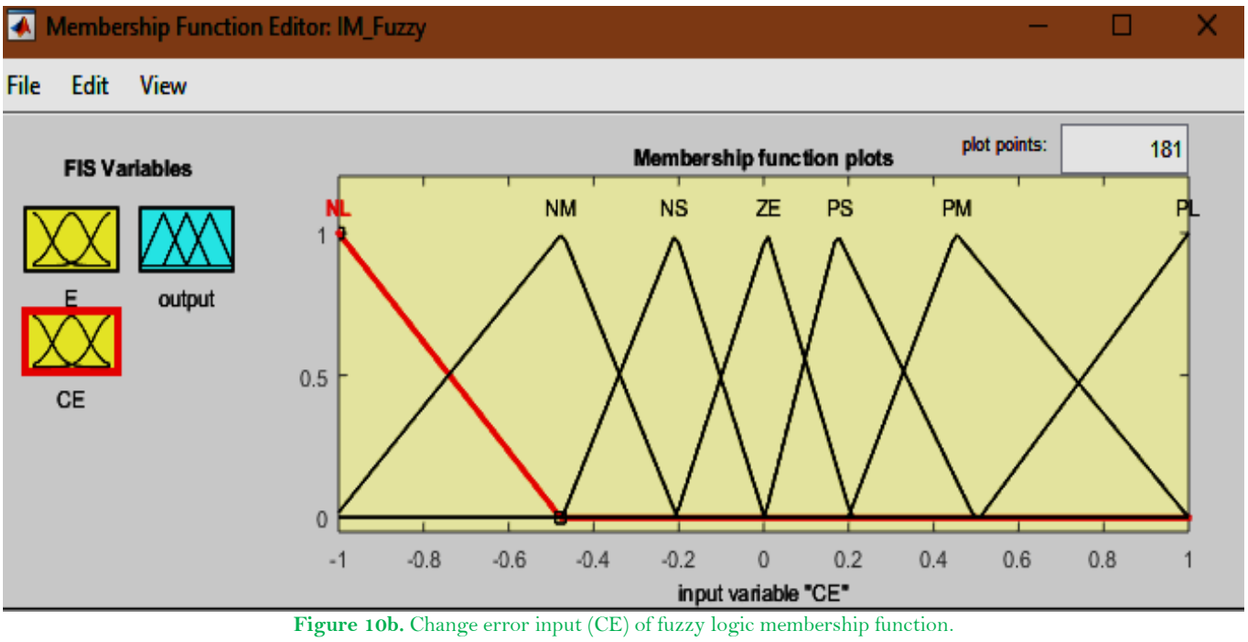

Figure 10b. Change error input (CE) of fuzzy logic membership function.

The "Change in Error" (CE) input of a fuzzy logic membership function modifies the parameters that define the shape and position of its fuzzy sets. The goal is to optimize the fuzzy logic controller's performance by adjusting how the "change in error" is interpreted. Triangular fuzzy set membership functions were selected for implementation as shown in Figure 10c.

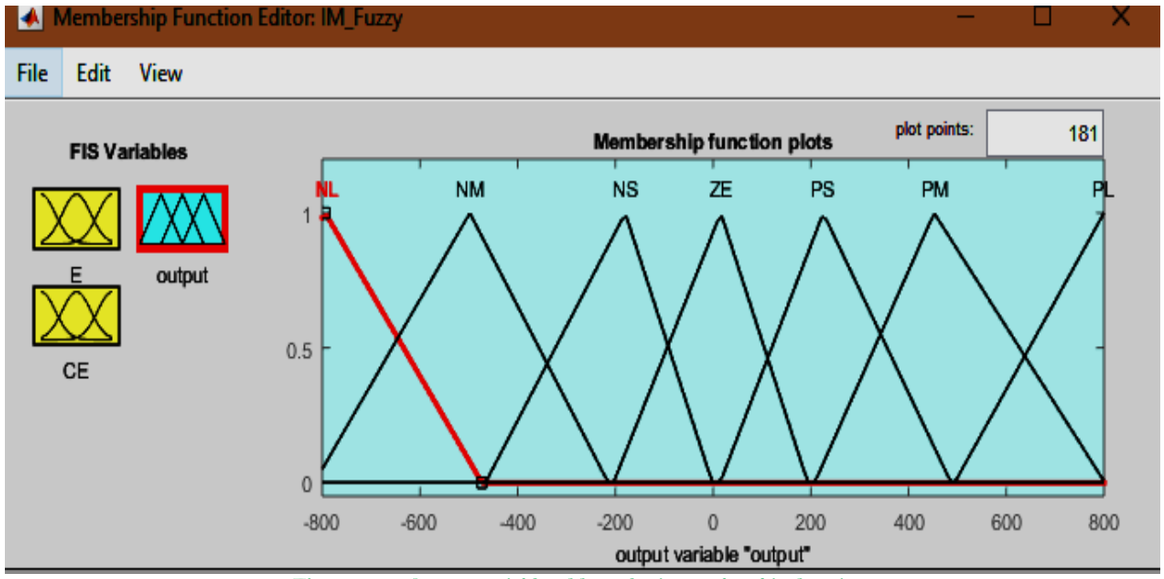

Figure 10c. Output variable of fuzzy logic membership function.

In the diagram, the output variable of a fuzzy logic membership function quantifies the degree of belongingness of a crisp input to a fuzzy set, serving as a crucial component in both fuzzification and defuzzification processes within a fuzzy logic system. This represents the extent to which the input (0 and 1) value belongs to a particular fuzzy set.

3.6. Fuzzy-PID Design

In the Fuzzy-PID control system, the new proportional control is called GE (i.e. product of the new proportional gain K'_p and error), the new derivative control is called GCE (i.e. product of the new derivative gain K'_d and change in error), and the new integral control is called GIE (i.e., product of new integral gain K'_i and integration of error. GU is the product of K_p and the control variable. The numerical values of the modified PID gains for the Fuzzy-PID controller are defined as follows:

$$\left.\begin{aligned} K'_p &= 3.58 \\ K'_d &= \frac{K_d}{K_p} = 3.47e03 \\ K'_i &= \frac{K_i}{K_p} = 0.000922 \end{aligned}\right\} \quad (29)$$

Therefore, with the modified PID parameters integrated with the designed FLC model, a Fuzzy-PID-based control system was developed as shown in Figure 11.

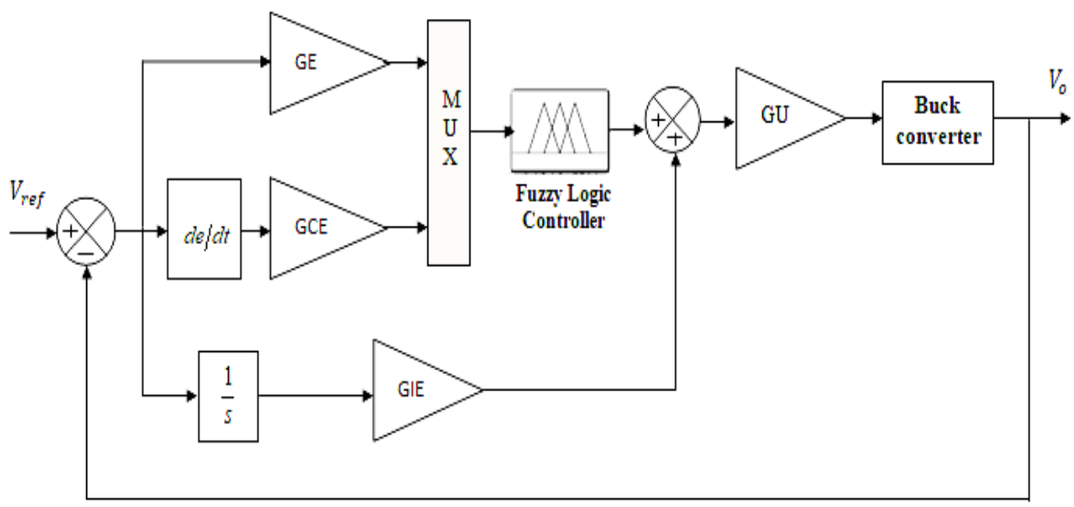

Figure 11. Fuzzy-PID control system.

3.7. Simulation Parameter and Design Flowchart

The parameters of the buck converter are listed in Table 1. These parameters were entered into embedded blocks of the MATLAB/Simulink model developed for a computer simulation test conducted to examine the dynamic responses of the cascaded control system for the buck converter. The design flow chart is shown in Figure 11.

Table 1. Buck converter parameters.

Definition	Symbol	Value
Input voltage	V_g	36 V
Set-point voltage	V_{ref}	12 V
Resistance	R	6 Ω
Inductor	L	1 mH
Capacitor	C	100 µF
Duty cycle	D	1/3
Switching frequency	F_s	40 kHz

Source: Jabari et al. [14].

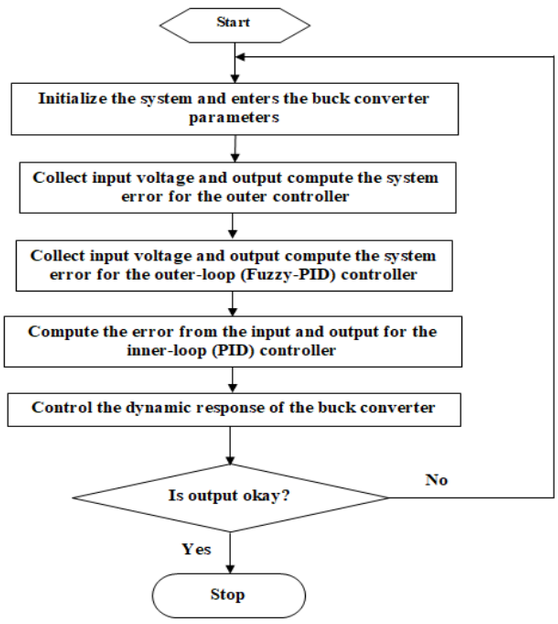

Figure 12. System Implementation Flowchart.

4. Simulation Results and Discussion

4.1. Response of Open-Loop Buck Converter Control System

The small-signal (dynamic) model of the buck converter, developed as shown in Figure 12 and described by the transfer function of the output voltage in Equation 1, the parameters in Table 1 were entered to analyze the step response. The simulated waveform for the step response of the buck converter when operated with the controller in control-loop state is shown in Figure 14. The resulting Bode plot for the system stability analysis and frequency response is shown in Figure 1.

4.2. Step Response of PID Control System

In this section, the output of the DC-DC buck converter was compensated with a PID controller, as shown in Figure 13. The resulting step response of the output voltage and the Bode plot are shown in Figure 13 and Figure 14, respectively.

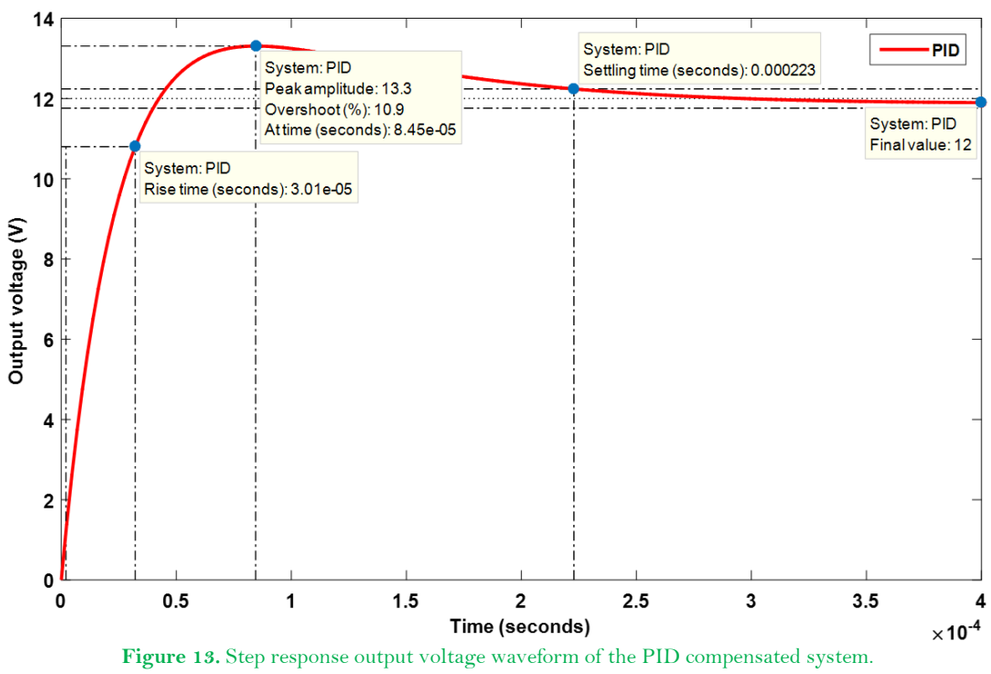

Figure 13. Step response output voltage waveform of the PID compensated system.

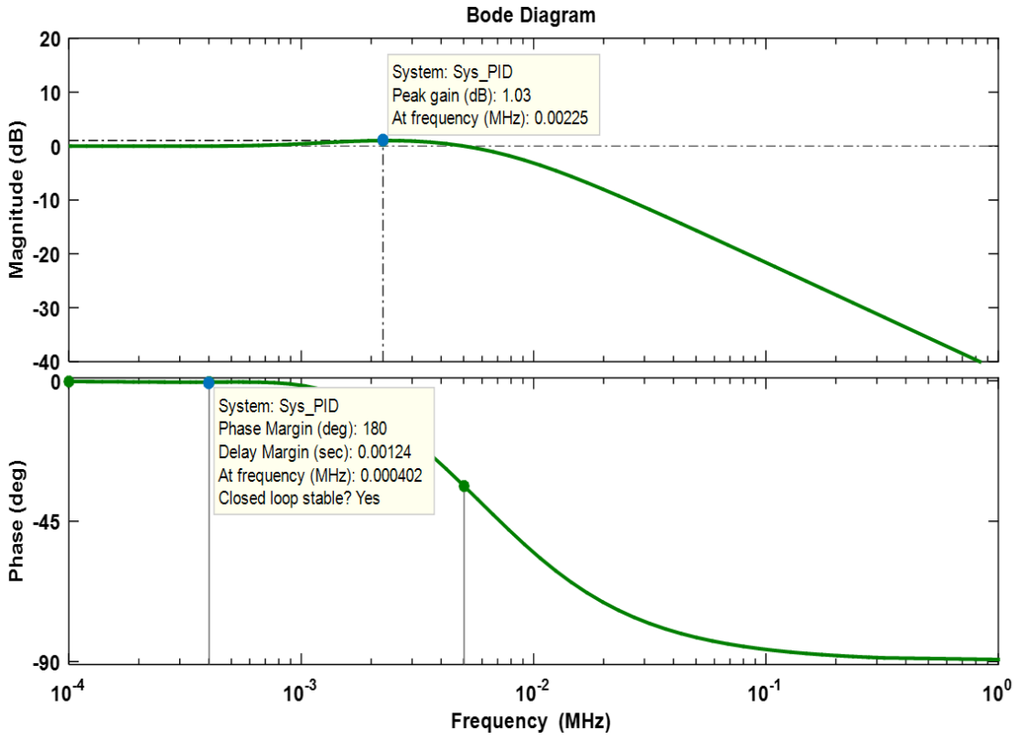

Figure 14. Simulated Bode waveform of PID control buck converter.

The PID-controlled DC-DC buck converter's output voltage was evaluated in the time domain, considering rise time, settling time, peak time, and overshoot, which are essential parameters for analyzing transient response. In Figure 13, it is evident that the step response of the converter shows better stability than the uncompensated open-loop system, with reduced overshoot. Additionally, the application of the PID controller resulted in a faster response and shorter convergence to steady state, as indicated by the rise time and settling time listed in Table 2. The simulated Bode plot of the PID-controlled buck converter demonstrated improved stability, with a reduced peak gain of 1.03 dB at 2.25 kHz. A phase margin of 180 degrees was achieved at 402 Hz.

Table 2. PID-controlled buck converter transient response.

System state	Rise time (s)	Settling time (s)	Peak time (s)	Overshoot (%)	Final value (V)
Open loop	4.05e-04	0.00443	0.00105	42.3	12
PID control	3.01e-05	0.000223	8.45e-05	10.9	12

4.3. Response of Buck Converter with Cascade Fuzzy-PID and PID Controllers

The proposed multistage control system for the DC-DC buck converter, utilizing Fuzzy-PID and PID controllers and called the cascade control system (CC.sys), is evaluated in this section. The analysis primarily focuses on the transient response of the output voltage within the time domain. Additionally, the Bode plot of the system is presented to illustrate its frequency response. The transient response and Bode plot are shown in Figure 13 and Figure 14.

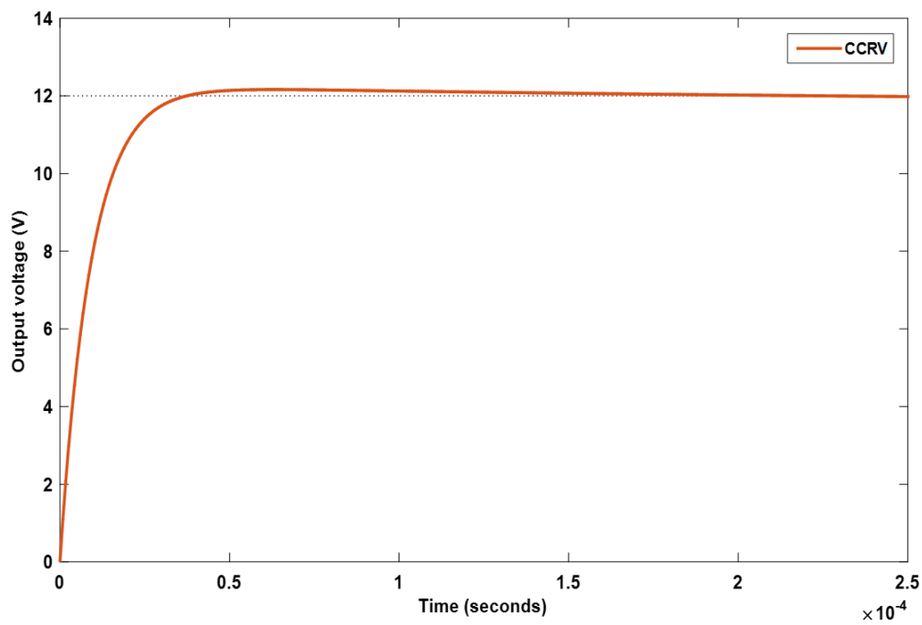

Figure 15. Step response output voltage waveform of the cascade control system.

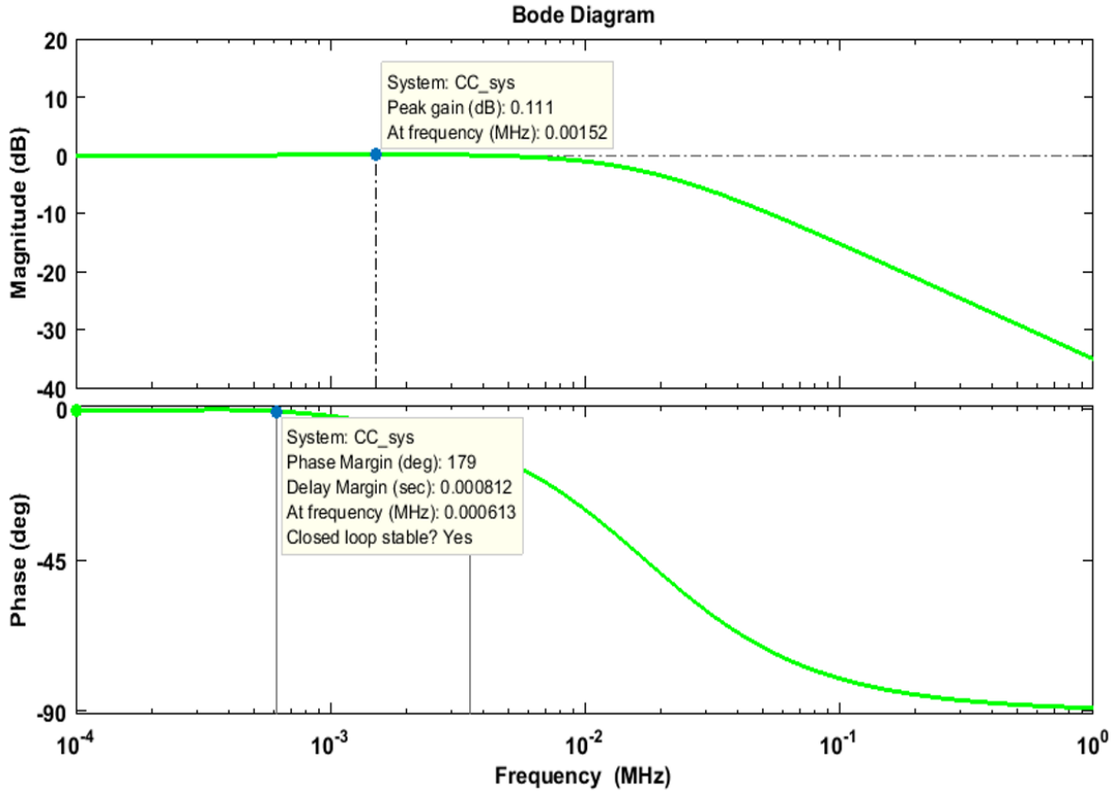

Figure 16. Simulated Bode waveform of cascade control buck converter.

The numerical values of the time domain parameters of the Fuzzy-PID and PID cascade control response voltage (CCRV) of the buck converter (Figure15) are listed in Table 3.

Table 3. Time domain characteristics of the transient response of the cascade system.

Parameter	Value
Rise time	1.88e-05 s
Settling time	3.02e-05 s
Peak time	6.29e-05 s
Overshoot	1.36%
Final value	12 V

The cascade control system based on fuzzy intelligent and PID controllers for the DC-DC buck converter presented a simulated waveform in Figure 16. The results indicated improved transient response performance, as evidenced by the evaluation of the system's response in terms of rise time, settling time, peak time, and overshoot, demonstrating enhanced control efficiency, as in Table 3. From the table, it is clear that the introduction of the designed cascade control system improved the transient response of the converter's output voltage. Further analysis in terms of frequency response, conducted using the Bode plot, revealed that the proposed system offered better stability than the PID control system, as evidenced by the reduced peak gain (0.111 dB) at a frequency of 1.52 kHz, as shown in Figure 16.

4.4. Designed Cascade Control Robustness Test

This section presents the robustness test of the designed cascade control system incorporating a fuzzy intelligent algorithm with PID. The analysis covers the robust evaluation of the DC-DC buck converter when the cascade controller was operationalized and integrated into the control system.

The section offers valuable insights into the adaptability and performance viability of the DC-DC buck converter in various operational scenarios through MATLAB simulations. Two basic scenarios were conducted, considering different input voltages and load conditions. This analysis enhances understanding of the converter's performance characteristics. Examining the response of the cascade-controlled converter to different operational parameters provides significant insights into its capabilities and limitations.

Table 4. Cascade controlled buck converter transient response for different inputs.

System state under loading	Rise time (s)	Settling time (s)	Peak time (s)	Overshoot (%)	Final value (V)
CCRV (6 Ω)	1.88e-05	3.02e-05	6.29e-05	1.36	12
CCRV (7.2Ω)	1.21e-04	1.45e-03	3.28e-04	18	12
CCRV (4.8 Ω)	2.13e-05	3.46e-05	6.99e-05	1.11	12

The transient response analysis of the cascade-controlled converter reveals vital information about the performance of power electronic systems, which is common among electrical and electronic devices. Looking at Table 4, it is evident that an increase in load causes the transient response of the converter's output voltage to overshoot the setpoint by a significant 18%. This demonstrates how increasing load impacts system performance, potentially leading to instability over time due to overloading. However, the cascade controller ensures that the desired voltage is maintained at the output.

The Bode plots for 7.2 Ω and 4.8 Ω loads are shown in Figures 17 and 18. These plots compare the stability performance of the designed cascade control buck converter under different load conditions.

Table 4 shows the frequency response performance of the cascade control converter under different loading.

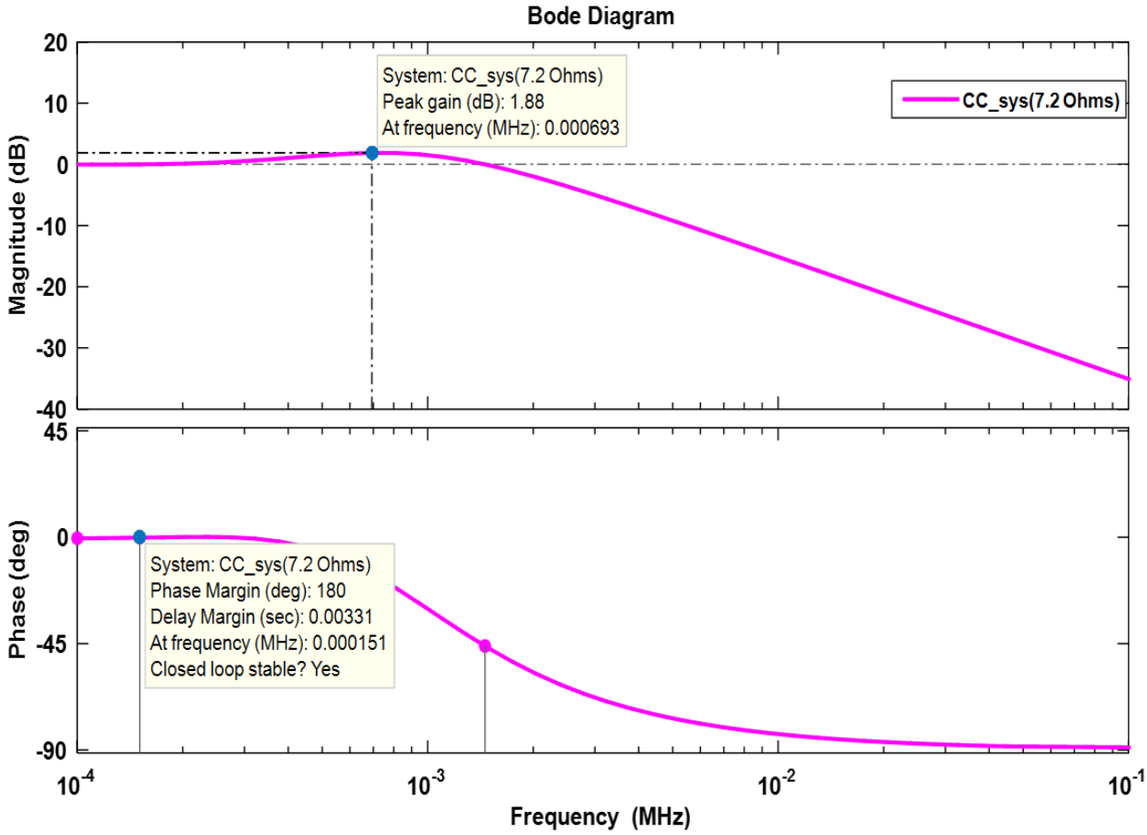

Figure 17. Simulated Bode plot of cascade control buck converter with load 7.2 Ω.

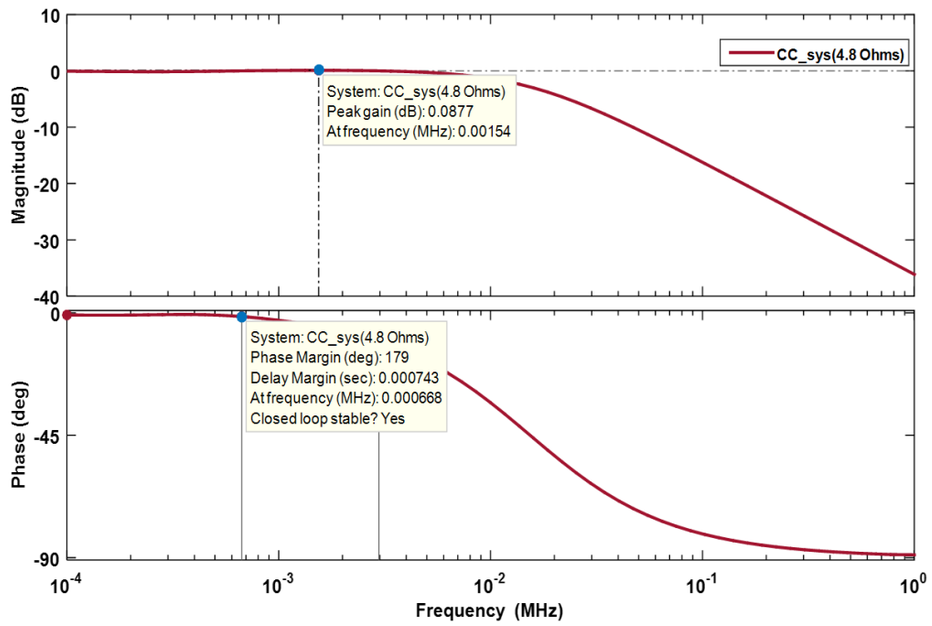

Figure 18. Simulated Bode plot of cascade control buck converter with load 4.8 Ω.

Table 5. Bode analysis of the cascade control buck converter under different loads.

System state under loading	Peak gain (dB)	Gain margin (dB)	Phase margin (deg.)	Bandwidth (Hz)
CC_sys (6 Ω)	0.111	Infinite	179	1.79×10^4
CC_sys (7.2 Ω)	1.88	Infinite	180	2.31×10^3
CC_sys (4.8 Ω)	0.0877	Infinite	179	1.59×10^4

In evaluating the performance of controllers in the frequency domain, fundamental parameters such as peak gain, gain margin, phase margin, and bandwidth are essential. Table 5 presents the frequency response domain performance indices for various loading conditions of the cascade control converter. The table, which reflects the Bode plots under different loading conditions, shows that the cascade controller exhibited the best stable frequency response when the load was 6 Ω. It can be concluded that the system demonstrated a certain level of robustness, considering the phase margin values.

4.5. Performance Comparison with PID Control System

This section compares the intelligent aid cascade control system with the classical PID control system, which has been widely implemented in previous literature. Figure 4.11 displays the transient response comparison of the open-loop, PID, and the designed cascade control system, using the standard parameters of the DC-DC buck converter listed in Table 1.

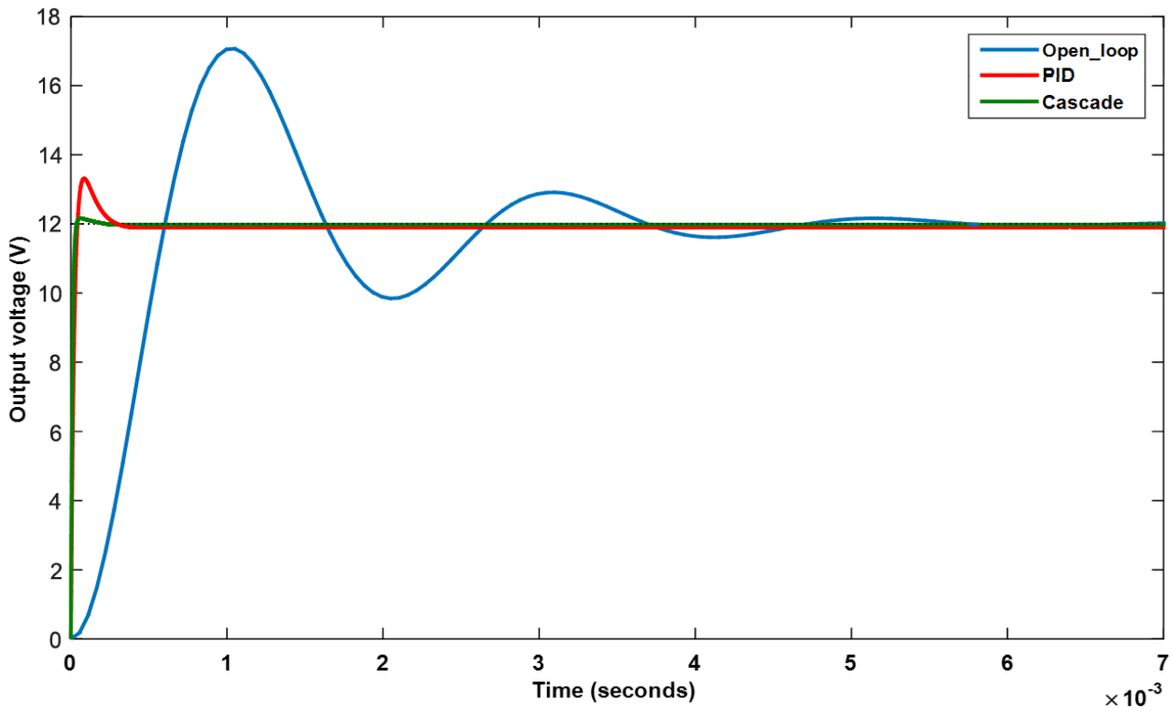

Figure 19. Step response comparison of different control systems.

The numerical evaluation of the step response waveforms in Figure 18 is presented in Table 5.

Table 6. Performance comparison of buck converter transient response.

System state	Rise time (s)	Settling time (s)	Peak time (s)	Overshoot (%)	Final value (V)
Open loop	4.05e-04	0.00443	0.00105	42.3	12
PID control	3.01e-05	0.000223	8.45e-05	10.9	12
Cascade	1.88e-05	3.02e-05	6.29e-05	1.36	12

The transient response performance of the buck converter under different control conditions, as listed in Table 6 and shown in Figure 19, revealed that the cascade control buck converter offered the best results. It provides the fastest response (rise time), the quickest convergence to steady state (settling time), the shortest time to reach peak value (peak time), and the most stable, smooth response (overshoot).

5. Conclusion and Recommendations

5.1. Summary of Discussion

This work presents a DC-DC buck converter circuit that combines cascade control techniques based on Fuzzy-PID and PID algorithms for improved transient response performance. A DC-DC buck converter was designed, and Fuzzy-PID and PID controllers were incorporated into the system to enhance transient response in terms of rise time, settling time, and overshoot, with high voltage/power transfer efficiency. Simulations were conducted in MATLAB/Simulink to verify the system's effectiveness, and the results were evaluated against key parameters in the transient response time and frequency domains. A comparison test with a classical cascade control system was also performed.

5.2. Conclusion

Conclusively, the use of cascade controllers in power electronics converters embedded with fuzzy logic systems offers significant improvements in dynamic response and stability, including overshoot, settling time, and frequency. The results of this study demonstrate the effectiveness of the fuzzy logic control system embedded in the PID cascade controllers' strategy, which can be applied to various power converter topologies and applications, such as electric vehicles, renewable energy, and consumer electronics.

5.3. Contribution to Knowledge

The cascade combination of Fuzzy-PID and PID controllers to enhance the transient response time and frequency domain performance of a DC-DC buck converter has been realized.

In this work, the dynamic challenges common with power electronic systems, especially during loading, were demonstrated through computer-based simulations.

5.4. Recommendations/ Future Work

In future studies, efforts should be made to explore other schemes or approaches designed to extend and improve the findings of this work.

Hardware implementation is urgently needed to validate the effectiveness of the cascade control technique in practical applications. This will help bridge the gap between theoretical investigation and real-world application. Other control strategies, such as adaptive controllers and multi-objective optimization methods, should be investigated alongside the designed cascade control scheme in this work.

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